POROSITY EFFECTS ON COPLANAR WAVEGUIDE POROUS SILICON INTERCONNECTS

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Abstract — **Oxidized porous silicon (OPS) has the potential to produce low loss designs for high-density RF passive and CMOS integrated circuits. Herein are findings on porosity effects on finite ground coplanar waveguide (FGCPW) lines printed on OPS material up to 50 GHz. At 51% porosity, measured effective dielectric constant data ($\varepsilon_{r,eff}$) is approximately 2.8 and is consistent with Bruggeman models. For similar low (low-rho) and high (high-rho) resistivity silicon designs, OPS attenuation (dB/cm) exhibits 78% less loss than low-rho designs with 1.5 and 9.5% less than and greater than, the high-rho design at 10 and 20 GHz, respectively. Furthermore, wideband 50-ohm impedance matching is achieved. These findings, therefore, support consideration of oxidized porous silicon for RFIC design.**

I. INTRODUCTION

Development of compact integrated designs that combine data processing and communications into a single unit require RF designers to contemplate design approaches that are complementary to other circuits, like switches and processors. In doing so, one may include micro-electro-mechanical (MEMs) devices for switching and complementary metal oxide semiconductor (CMOS) for digital integrated circuit (IC) processing that must be combined with monolithic microwave integrated circuit (MMIC) approaches. Recent demonstrations of silicon RF MMIC designs [1-2] to complement existing CMOS and MEMs circuits motivate development of approaches that allow CMOS grade silicon to be considered for high frequency passives.

Several design conflicts arise when silicon substrates are considered for active and passive circuit design. While standard IC processing methods are common to each circuit type (e.g. RF, CMOS, and MEMs), there are two main dilemmas. One is how to optimize dielectric layer use as masks or isolation and passivation layers in MEMs and in electronic devices, respectively. Careful assessment of process design specifications and steps will alleviate many of these concerns. The other, and perhaps most important to the RF designer, is how to address the conflicting substrate resistivity requirements for high electron mobility and high isolation in high-speed transistors and passive component design, respectively.

Porous silicon, described in [3-4] can satisfy both and has been recently utilized in [5] by the authors of [4]. By anodizing the low resistivity silicon substrate, high conduction areas suitable for device development can be integrated with low conduction domains (e.g. porous silicon). For RF passive development, early examples include, high quality factor RF lumped elements (published as high as 29 at 7GHz [3]) and coplanar waveguide attenuation losses as low as 3.26 dB/cm at 10 GHz [4]. From a design perspective however, limited data is available on RF electrical properties as a function of porosity that is important for RF design, while significant research has been done on its use in isolating low frequency IC's and optical qualities for photonic applications.

Initial dielectric properties of capped oxidized porous silicon (OPS) up to 50 GHz were reported in [6]. Because porous silicon can offer complementary CMOS and MEMs fabrication capability, understanding its high frequency behavior can provide an important bridge in our current knowledge of this material at RF frequencies. In this article, we report findings on the effect of different porosity values on the microwave (1-50GHz) behavior of oxidized porous silicon films. Design and simulation for the finite ground coplanar waveguides (FGCPW) is presented. Comparison of the dielectric constant to existing complex material models is discussed, and the effect of porosity on the material dielectric constant is presented. Finally, attenuation curves and matching capabilities are shown.

II. FABRICATION AND DESIGN

Porous silicon is formed by anodization using the cell described in [6]. Lightly doped 10-25 Ω-cm p-type (boron) silicon wafers with (100) crystal plane orientation and a thickness of 525 μm are anodized at 10 mA/cm^2 in an HF mixture (49% HF:pure ethanol 5:3). The backside of the wafer is ion implanted to insure an ohmic contact from the secondary electrode to the wafer. The resulting samples have porosities of 51% and 65% (determined gravimetrically) and film thickness of approximately 34 and 75 μm respectively (determined by scanning electron

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micrograph). An HF mixture of 49% HF:pure ethanol 3:7 produces an 85% porosity film of 20 μm.

Passivation is performed by rapid thermal oxidation (RTO) for 30 minutes at 350°C since oxidation is needed to terminate the dangling silicon bonds with a few monolayers of oxygen to make the material chemically stable in ambient [7]. The samples are capped with 4800Å of plasma-enhanced chemical vapor deposited (PECVD) silicon dioxide and metal adhesion layers are gold electroplated to 4 μm on Ti/Au seed layers.

Since porosity ultimately impacts the dielectric constant of the material, coplanar waveguide (CPW) circuits are chosen since the line impedance is weakly coupled to the substrate's dielectric constant. Simulation data in Ansoft's Maxwell 2D shows a near flat response between effective dielectric constant (ε_{eff}) and line impedance. In a low index material, for example, a substrate with ε_r of 3.9 at 10 GHz on a 24 μm thick substrate shows a dielectric constant variation for CPW dimensions of S+2*W = 71 μm between 2.6 and 2.5 for an impedance range of 27 and 103 Ω where S is the signal width and W is the gap width.

In this work, the bulk lossy silicon substrate also impacts the experimental characterization of these films. When the height of the substrate, h_{ops}, is less than the CPW gap, W, the electric fields penetrate the underlying host substrate (see Fig. 1(a)). For $h_{ops} > W$, Fig. 1(b), shows field confinement is dominant in the OPS film. The corresponding CPW line dimensions are S-W-W_g = 47-12-140 μm (signal, gap and ground plane width) for a 50 Ω impedance using an estimated relative dielectric constant value of 5.

III. RESULTS

Device S-parameter response is measured with an Agilent 8510C automatic network analyzer connected to a Cascade Microtech/Alessi RF1 microwave on-wafer probe station. Cascade Microtech GSG150 probes are used to perform the NIST's MultiCal TRL (Through-Reflect-Line) de-embedding calibration [9]. Each porosity sample contains distinct TRL calibration circuits.

A. Modeling vs. Experimental Dielectric constant evaluation

In this work the dielectric constant of various OPS films is determined for different film porosities. The dielectric constant is calculated from experimentally obtained phase data using equation (1)

$$\theta = \beta \cdot l = \frac{2\pi}{\lambda \cdot g} = \frac{2 \cdot \pi \cdot f \sqrt{E_{eff}}}{C} [Radians] \quad (1)$$

A reference porosity value is determined for a control wafer using a volumetric approximation. The porosity value is then used to predict an estimated value of film dielectric constant based on microwave measurement data. Two models are used to establish baseline values for the OPS dielectric constant versus porosity. The linear model in equation (2) produces a coarse estimate, while the Bruggeman [10] equation (3) reflects the more traditional calculation for composite materials, where $\varepsilon_{r,Air}$, $\varepsilon_{r,Si}$ and $\varepsilon_{r,OPS}$ are 1, 11.7 and the OPS dielectric constant, respectively. P is the film porosity. Film thickness is not included in this calculation.

$$\varepsilon_{r,OPS} = \varepsilon_{r,si} \cdot (1-P) + \varepsilon_{r,air} \cdot (P) \quad (2)$$

$$(1-P) \cdot \frac{\varepsilon_{r,Si} - \varepsilon_{r,OPS}}{\varepsilon_{r,Si} - 2 \cdot \varepsilon_{r,OPS}} + P \cdot \frac{\varepsilon_{r,Air} - \varepsilon_{r,OPS}}{\varepsilon_{r,Air} - 2 \cdot \varepsilon_{r,OPS}} = 0, \quad (3)$$

Fig. 2 plots experimental data versus linear (dashed) and Bruggeman (solid) predictions. For porosities below 65%, the data follows the Bruggeman model closely for thin (34 μm) and thick (75 μm) OPS films. At higher porosities, however, the results approach the coarse linear model. This film exhibits a more dense structure near the bulk material thereby resulting in a higher dielectric constant than expected. These issues are currently being investigated.

B. Film thickness effects

Experimental results for the CPW designs on various porosity substrates are shown in Fig. 3. For porous samples following the Bruggeman model, the effective dielectric constant decreases as the porosity increases, as expected. Note to compensate for the potential higher film density near the host substrate, the 65% porous film thickness is 75 μm, almost twice the 51% case. In [3], dramatic improvements in inductor quality factors (Q) around 7 GHz have been linked to substrate removal beneath films as thick as 100 microns. Furthermore, the modeled 57 Ω CPW response using [11] on layered lossless OPS (ε_r 3.44) and lossy (15 Ω-cm, ε_r 11.75) bulk silicon shows a decrease in $\varepsilon_{r,eff}$ from 2.38 to 2.15. As the OPS film height increases from 34 to 125 microns for a combined OPS/silicon height of 525 μm, the saturated $\varepsilon_{r,eff}$ value is 2.15 at 125 μm. This result is a 2 Ω increase in characteristic impedance.

To more accurately model the OPS, loss effects will be included. Careful attention will be given to the impact of locally defined losses in layered media and comparisons will be made to experimental data. Note that the network of porous silicon material is connected to the lossy bulk material at the interface. For very high porosities in lightly

doped substrates, the film morphology varies with depth, and is being investigated further to develop accurate models of RF behavior on thin porous films.

C. Attenuation and Matching Capability vs. Porosity

Fig. 4 compares the effect of porosity on the CPW line and contrasts this data to the performance of similar lines on low loss (< 1000 Ω-cm, ε_r=11.7) and lossy (10-25 Ω-cm, ε_r=11.7) silicon substrate (S-W-W_g of 33-18-140 μm). Since the design dimensions are quite narrow, conductor loss values can be diminished with wider electrode choices. For the 51% porosity film (shown by triangles), loss values are 2.69 and 4.09 dB/cm at 10 and 20 GHz. This reflects a 78% reduction in attenuation compared to the CMOS substrate design. Additional loss reduction is observed for the 85% case (1.88 and 2.78 dB/cm). Note the best attenuation estimates for the low loss silicon design would produce values of 2.73 and 3.70 dB/cm at 10 and 20 GHz, where the 85% OPS attenuation is at best 66 percent less than the low loss design for similar designs.

Smith chart data in Fig. 5(a) and (b) compares the impedance matching of a lossy 45 Ω silicon line to a 52 Ω OPS line respectively. The wideband (1-50 GHz) convergence of the interconnect impedance to the center of the smith chart indicates significant improvement of the OPS substrate loss compared to the lossy CPW design. This indicates that with suitable electrical parameter knowledge, this material can offer much needed improvements of RF passives to CMOS based designs.

IV. SUMMARY

Porosity values in OPS can provide important insight on the RF electrical response of this material. Data has been presented on the effect of porosity and film thickness as it relates to composite material models. Effective dielectric constant values saturate at 2.8 for middle range porosity, (51%). The OPS attenuation reduction is between 78-85% over the standard CMOS substrate. The highest porosity film (85%) indicates less attenuation to similar design in high-rho silicon. Finally, 50 GHz wideband impedance matching is demonstrated in the OPS substrate. The significant reduction in low resistivity material and matching via porous silicon makes this material suitable for RF applications.

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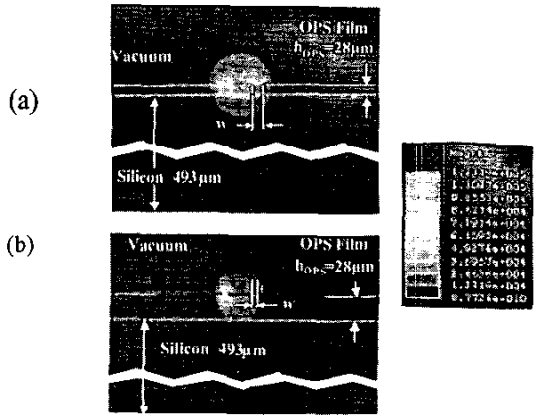

Fig. 1. Field plot of Maxwell 2D simulation @10GHz. Lossless OPS film $\varepsilon_r = 3.63$. Lossy bulk silicon $\varepsilon_r = 11.7$ and $\rho = 17\ \Omega$-cm (a) W=53 μm > h_{ops}. (b) W=12 μm < h_{ops}.

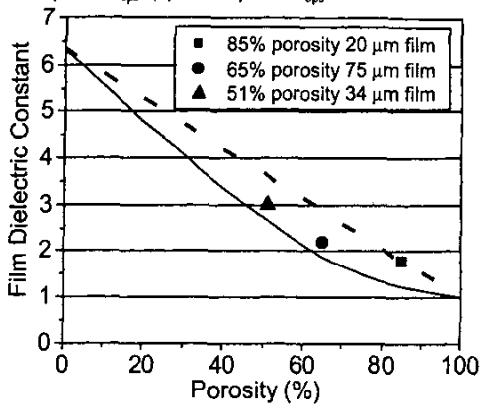

Fig. 2. Film dielectric constant as a function of porosity using the Bruggeman (solid line) and linear approximation (dashed line) and the various film samples tested @ 30GHz.

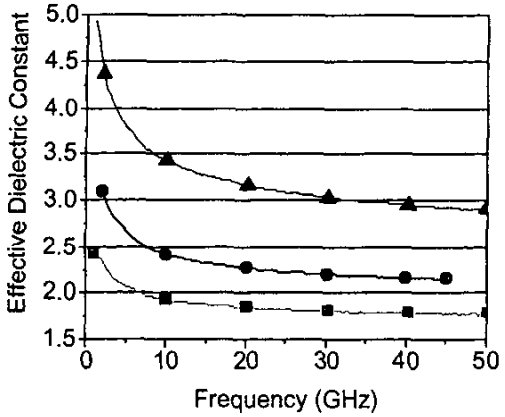

Fig. 3. Effective dielectric constant as a function of frequency for various porosity films. Symbols in Fig. 2.

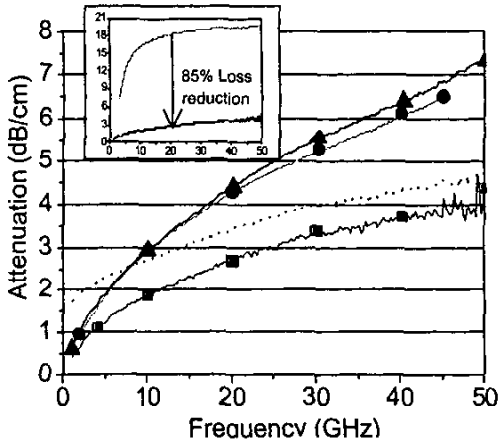

Fig. 4. Attenuation (dB/cm) as a function of frequency for various porosity films and high-rho silicon (dashed line). Symbols in Fig. 2. The insert curve shows attenuation in low-rho silicon (top) vs 85% porosity film (bottom).

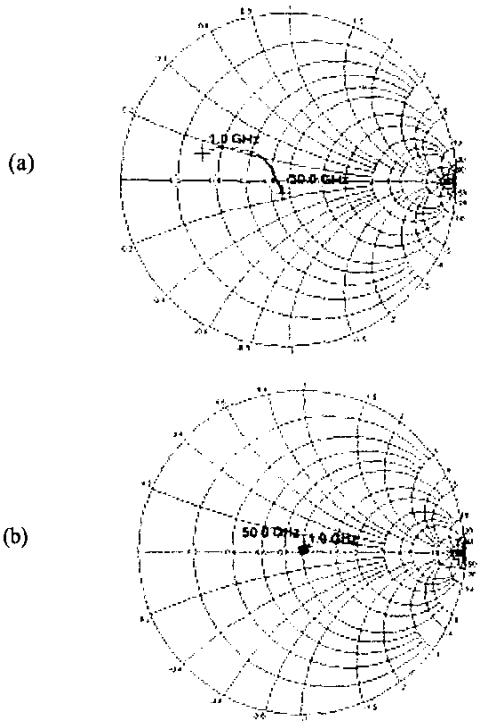

Fig. 5. (a) Smith chart of a 47 Ω circuit on CMOS grade silicon 10-25 Ω-cm and 521 μm. (b) Smith chart of a 52 Ω circuit on a rooted OPS film 20 μm thick and 85% porosity. Results based on MultiCal TRL calibration.